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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,935	11/18/2003	Kazuhiko Maeda	1035-483	3704
23117	7590	09/13/2007	EXAMINER	
NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203				NGUYEN, JIMMY H
ART UNIT		PAPER NUMBER		
		2629		
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09/13/2007		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,935	MAEDA ET AL.	
	Examiner	Art Unit	
	Jimmy H. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 September 2007.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-3,5,7-18 and 20 is/are rejected.
 7) Claim(s) 4,6 and 19 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 04 September 2007 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____. 	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/4/2007 has been entered. Claims 1-20 are currently pending in the application. An action follows below:

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 19 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to claim 19, when this claim is read together with independent claim 17, this claim recites limitations, (i) "circuits other than unit circuits of the first shift register are disposed in the physical spaces between adjacent unit circuits of the first shift register" presently recited in lines 6-7 of claim 17 and (ii) "wherein the other circuits comprise unit circuits for a second shift register different from the first shift register" presently recited in lines 2-3 of claim 19. Note that the limitation (i) may imply "**plural** other circuits are disposed in a **single** physical space between two adjacent unit circuits of the first shift register". In other words, the limitations (i)

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and (ii) may imply “**plural** unit circuits for a second shift register are disposed in a **single** physical space between two adjacent unit circuits of the first shift register”, which was not supported in the original disclosure.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-10 and 12-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Azami (US 6,702,407 B2).

As to claims 1, 2, 8-10, 13, 17, and 20, the claimed invention may be read in the Azami reference as follows: Azami discloses a **display device** (an active matrix image display device; see col. 6, line 52 and Fig. 30), comprising a **plurality of data signal lines** (source signal lines 104/SL; see Fig. 30; col. 1, line 35; col. 7, line 37); a **plurality of scanning signal lines** (gate signal lines 105; see Fig. 30; col. 1, line 36) intersecting with the data signal lines (104/SL); pixels (Fig. 30, col. 1, line 39) provided for each pair of the data signal lines and the scanning signal lines; a **scanning signal line driving circuit** (a gate signal line driving circuit 102; see Fig. 30; col. 1, line 31) for driving the scanning signal lines; and a **data signal line driving circuit** (a source signal line driving circuit 101; see Figs. 3 and 30; col. 1, line 30) comprising a **sampling section** (a section including first and second latch portions, P/S conversion circuits, D/A conversion circuit, and a source line selecting circuits; see Fig. 3) for driving a **plurality of**

data signal lines (SL) by sampling image data from an image signal according to a selection signal (output of a FF; see Fig. 3) sequentially outputted from a shift register block (a shift register portion; see Fig. 3), so as to transfer the image data to the data signal lines, and **a shift register block** (a shift register portion).

Azami further teaches the **shift register block** (a shift register portion; see Fig. 3) comprising a **first shift register** (a first shift register comprising, e.g., first 4 flipflop (FF) circuits; see Fig. 3) and a second shift register (a second shift register comprising next 4 FF circuits and inverters and NAND gates and their connections associated with the first four FF circuits; see Fig. 3). Azazi teaches the first shift register comprising **4 unit circuits** (4 FF circuits) spaced-apart cascade-connected; outputting an input signal (a start pulse SP; see Fig. 3) in response to a clock signal (CLK; see Fig. 3, col. 6, lines 64-67); and sequentially outputting a selection signal from output-stages comprised of the unit circuits (see Fig. 3, col. 6, lines 64-67). Azami further teaches the unit circuits (FF circuits) of the first shift register being linearly disposed so that physical spaces are provided between adjacent pairs of the unit circuits (see Fig. 3). Azami further teaches **first (or other) circuits** (**each circuit including an inverter, an NAND, and their connections**; see Fig. 3) different from the unit circuits (first 4 FFs) of the first shift register, disposed in the physical spaces between adjacent unit circuits (FFs), and having outputs, which are not supplied to any of the unit circuits (FF circuits) of the first shift register (see Fig. 3). Accordingly, all limitations of these claims are read in the Azami reference.

As to claims 3-5, 18 and 19, as discussed above, each first (or other) circuit including an inverter, an NAND, and their connections (see Fig. 3) may be considered as a processing circuit

which used output of one of the unit circuits of the first shift register; a unit circuit for a second shift register different from the first register; or a waveform processing circuit.

As to claims 6 and 7, Azami teaches signal paths (paths for transmitting clock signals to each FF circuit of the first shift register; see Fig. 3) for the first shift register provided on the **top side** of a circuit alignment of the unit circuits of the first and second shift registers and signal paths (paths for transmitting the output signals from the inverters and NAND gates to the first latch portion; see Fig. 3) for the second shift register provided on the **bottom side** of a circuit alignment of the unit circuits of the first and second shift registers (see Fig. 3).

As to claim 12, Azami teaches the image signal being digital signal (DR0-DR2, DG0-DG2 and DB0-DB2; see Fig. 3; col. 7, lines 10-14) and the first circuit (a circuit including an inverter, an NAND, and their connections; see Fig. 3) comprising an output circuit, which use outputs of the unit circuits of the first shift register (see Fig. 3).

As to claims 14-15, Azami teaches the data signal line driving circuit and the scanning signal line driving circuit formed on a substrate on which the pixels are formed (see col. 10, lines 33-42); the pixels, the data signal line driving circuit, and the scanning signal line driving circuit including active elements (TFTs), respectively, each of which is made of a polysilicon thin film transistor (see col. 10, lines 33-42 and col. 15, lines 6-27).

As to claim 16, Azami teaches the active elements formed on a glass substrate at a process temperature of not more than 600°C (see at least at col. 10, line 56 through col. 67; col. 11, lines 39-46; col. 15, lines 21-27).

6. Claims 1-10 and 13-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Washio et al. (US 6,724,361 B1), hereinafter Washio.

As to claims 1, 2, 8-10, 13, 17, and 20, the claimed invention may be read in the Washio reference as follows: Washio discloses a **display device** (an image display device 11; see Fig. 2; col. 10, line 4), comprising a **plurality of data signal lines** (data signal lines SL₁-SL_n; see Fig. 2; col. 10, line 11); a **plurality of scanning signal lines** (scanning signal lines GL₁-GL_n; see Fig. 20; col. 10, lines 8-9) intersecting with the data signal lines (SL); pixels (16) (see Fig. 2, col. 10, line 12) provided for each pair of the data signal lines and the scanning signal lines; a **scanning signal line driving circuit** (a gate signal line driving circuit 13; see Fig. 2; col. 10, line 19) for driving the scanning signal lines; and a **data signal line driving circuit** (a data signal line driving circuit 14; see Fig. 2; col. 10, line 29) comprising a **sampling section** (18) (see Fig. 2) for driving a plurality of data signal lines (SL) by sampling image data from an image signal according to a selection signal (output of a FF; see Fig. 3) sequentially outputted from a **shift register block** (a shift register 1/27; see Figs. 2 and 11), so as to transfer the image data to the data signal lines, and a shift register block (1/27) (see col. 10, lines 28-38).

Washio further teaches the **shift register block** (27) comprising a **first shift register** (a first shift register comprising, e.g., first 4 flipflops (FFs) 23; see Fig. 11) and a second shift register (a second shift register comprising next 4 FFs 23 and inverters 24 associated with the first four FF circuits; see Fig. 11). Washio teaches the first shift register comprising **4 unit circuits** (4 FFs 23) spaced-apart cascade-connected; outputting an input signal (a signal inputted in S terminal of the first FF 23; see Fig. 11) in response to a clock signal (SCK/SCKB; see Fig. 11, col. 12, lines 55-67); and sequentially outputting a selection signal from output-stages comprised of the unit circuits (23) (see Fig. 11, col. 15, line 59 through col. 16, line 21). Washio further teaches the unit circuits (FFs 23) of the first shift register being linearly disposed so that

physical spaces are provided between adjacent pairs of the unit circuits (23) of the first shift register (see Fig. 11). Washio further teaches **first (or other) circuits (each circuit including an inverter 24; see Fig. 11)** different from the unit circuits (23) of the first shift register, disposed in the physical spaces between adjacent unit circuits (23), and having outputs, which are not supplied to any of the unit circuits (23) of the first shift register (see Fig. 11). Accordingly, all limitations of these claims are read in the Washio reference.

As to claims 3-5, 18 and 19, as discussed above, the first (or other) circuit (24) (e.g., **the second inverter 24** shown in Fig. 11) may be considered as a processing circuit which uses output of the first unit circuit (23) of the first shift register; a unit circuit for a second shift register different from the first register; or a waveform processing circuit.

As to claims 6 and 7, Azami teaches **signal paths** (paths for transmitting set signals to Sbar terminals to the first four FFs 23 or output signals Q from the first four FFs 23; see Fig. 11) for the first shift register provided on the **top side** of a circuit alignment of the unit circuits of the first and second shift registers and **signal paths** (paths for transmitting the reset signals R to the R terminal of the next 4 FFs of the second shift register; see Fig. 11) for the second shift register provided on the **bottom side** of a circuit alignment of the unit circuits of the first and second shift registers (see Fig. 11).

As to claims 14-15, Washio teaches the data signal line driving circuit and the scanning signal line driving circuit formed on a substrate on which the pixels are formed (see col. 38, lines 20-22; col. 41, lines 1-4); the pixels, the data signal line driving circuit, and the scanning signal

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line driving circuit including active elements (TFTs), respectively, each of which is made of a polysilicon thin film transistor (see col. 17, lines 37-43).

As to claim 16, Washio teaches the active elements formed on a glass substrate at a process temperature of not more than 600°C (see at least at col. 18, lines 31-42; col. 21, lines 27-36; and col. 41, lines 5-9).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Azami.

As to claim 11, Azami teaches that the circuit (a circuit including an inverter, an NAND, and their connections; see Fig. 3) different from the unit circuits comprises a waveform shaping circuit, a buffer circuit, or a sampling circuit, which uses outputs of the unit circuits (see Fig. 3). Azami further teach the driving system of the source signal line driving circuit including an analog system and a digital system (see col. 1, lines 43-47); therefore, while Azami does not exemplify that the image data being an analog mage data, but it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify the source signal line driving circuit of Azami to drive an analog image data since the image data can be represented by either one of them and it would not bring any unexpected result.

9. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washio.

As to claim 11, Washio teaches the first (or other) circuit (the second inverter 24) comprising a buffer circuit, which uses output of the first unit circuit (23) of the first shift register (see Fig. 11). Since the image signal must be either digital or analog and Washio is silent to the type of the image signal, Examiner, in the instant case, assumes the image signal of Washio is digital. Accordingly, Washio discloses all limitations of this claim except that Washio does not explicitly disclose the image signal being an analog signal, as presently claimed. However, while Washio does not exemplify that the image signal being an analog signal, but it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify the source signal line driving circuit of Washio to drive an analog signal since the image signal can be represented by either one of them and it would not bring any unexpected result.

As to claim 12, Washio teaches the first (or other) circuit (the second inverter 24) comprising an output circuit, which uses output of the first unit circuit (23) of the first shift register (see Fig. 11). Since the image signal must be either digital or analog and Washio is silent to the type of the image signal, Examiner, in the instant case, assumes the image signal of Washio is analog. Accordingly, Washio discloses all limitations of this claim except that Washio does not explicitly disclose the image signal being a digital signal, as presently claimed. However, while Washio does not exemplify that the image signal being a digital signal, but it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify the source signal line driving circuit of Washio to drive a digital signal since the image signal can be represented by either one of them and it would not bring any unexpected result.

Response to Arguments

10. Applicant's arguments, see pages 11-13 of the amendment filed on 9/4/2007, with respect to the drawing objection and rejections under 35 USC 112, first and paragraphs, in the Office Action dated 4/4/2007, have been fully considered and are persuasive in light of the amendments to claims and the replacement drawings. These objection and rejections are withdrawn.

11. With respect to the rejection under 35 USC 102(e) as being anticipated by Azami (US 6,702,407), Applicant argues that the inverters and NAND gates are not disposed in the physical space between adjacent flip-flops since Figure 3 of Azami is a schematic representation and does not reflect the relative physical arrangement of the various components shown therein. Examiner disagrees because at least the NAND gate receives a signal via a connection made between the two adjacent FFs (see Fig. 3) and the schematic representation is normally sketched similarly closed to the physical arrangement. Further, Applicant argues that assuming Fig. 3 showing a physical arrangement, the inverters and NAND gates are not disposed in the physical space between adjacent flip-flops. Examiner disagrees because Fig. 3 explicitly shows the inverters and NAND gates both disposed in the physical space between, e.g., the second and third flip-flops.

Conclusion

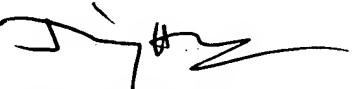
12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Friday, 6:30 a.m. - 3:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
September 10, 2007



Jimmy H. Nguyen
Primary Examiner
Technology Division: 2629



FIG. 17 Conventional Art

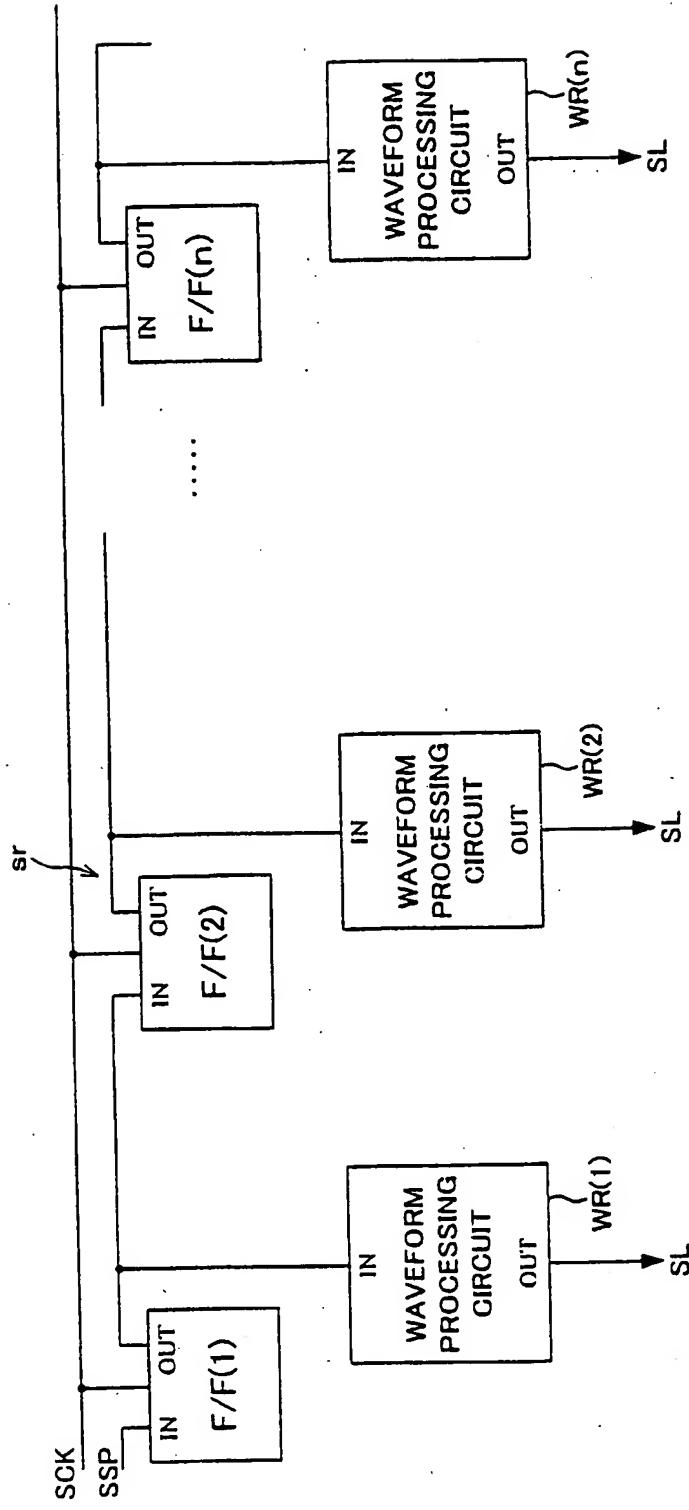


FIG. 18 Conventional Art

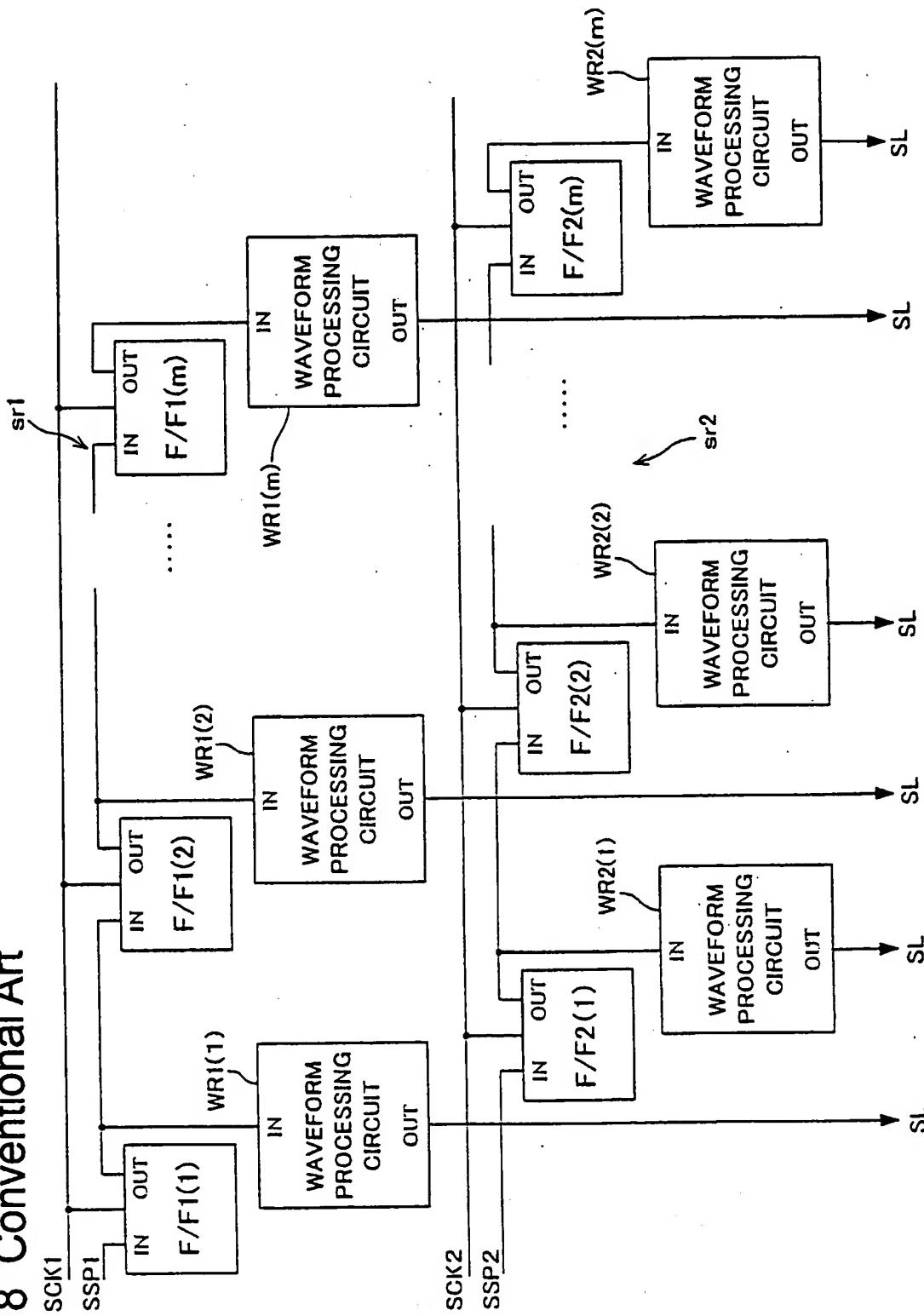


FIG. 19 Conventional Art

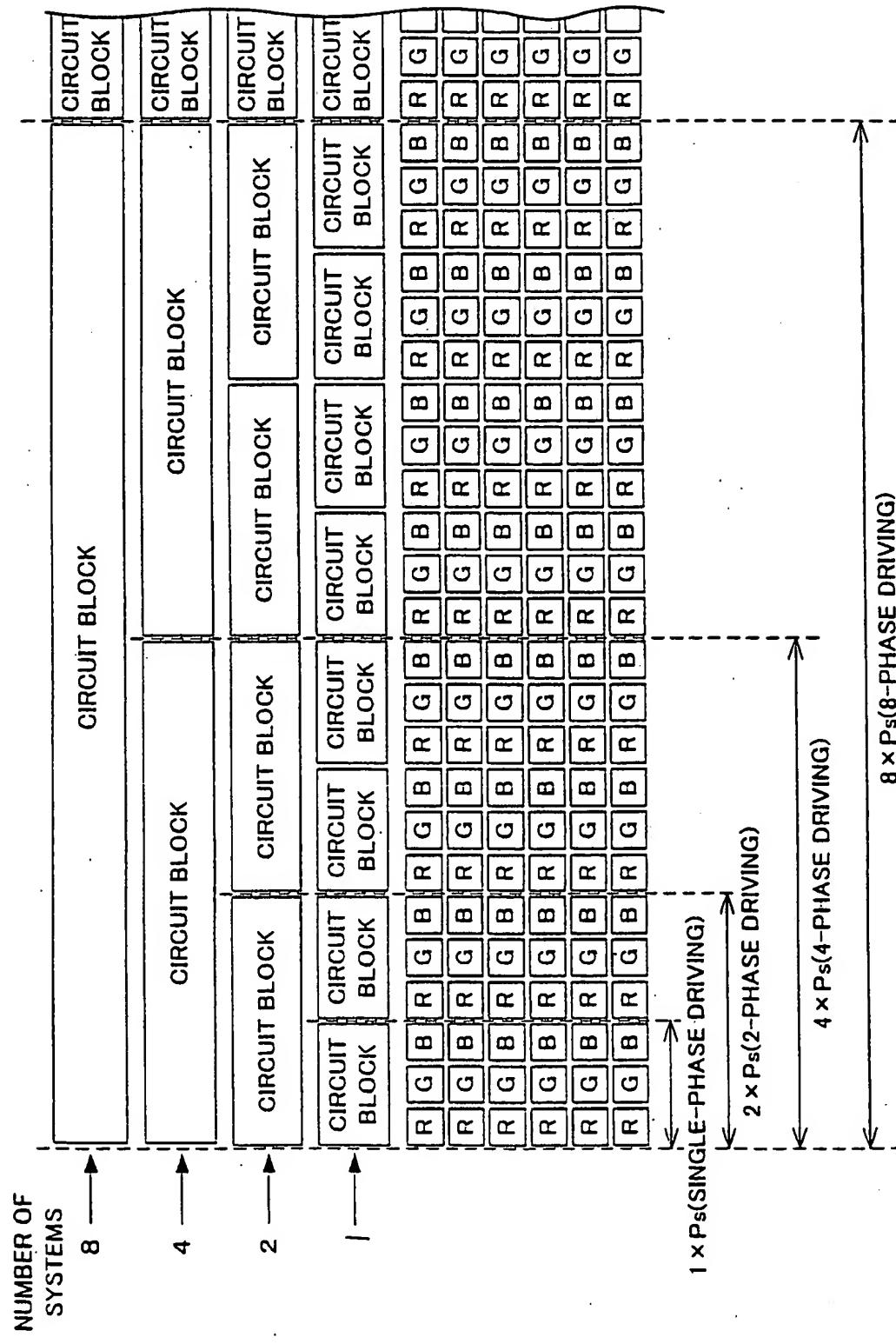


FIG.20 Conventional Art

